UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,421	06/30/2000	Thomas A. Tetzlaff	884.279US1	9595

21186 7590 03/15/2004

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
BRODA, SAMUEL	

ART UNIT	PAPER NUMBER
2123	3

DATE MAILED: 03/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/607,421	TETZLAFF, THOMAS A.	
	Examiner	Art Unit	
	Samuel Broda	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *7-15* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 16-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *7-15* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-6, 16-20, and 21-25, drawn to methods of initializing a computer-implemented simulation model, classified in class 703, subclass 22.

II. Claims 7-10, drawn to a computer-implemented method of evaluating an out node of a device model, classified in class 703, subclass 14.

III. Claims 11-15, drawn to a computer-implement method of simulating a self-resetting circuit, classified in class 703, subclass 14.

1.1 Inventions of Groups I, II, and III are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable.

In the instant case, the invention of Group I has separate utility such as initialization of any simulation model without regard to the apparatus or method being simulated. The invention of Group II has separate utility such as reducing the time to perform a device simulation through ignoring causes of unknown input values. The invention of Group III has separate utility such as modelling the behavior of a particular type of circuit at its activation.

These separate uses distinguishes the invention of each of Groups I, II, and III from one another. Therefore, the invention of each of Groups I, II, and III is a separately useable subcombination. See MPEP § 806.05(d).

1.2 Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification and/or recognized divergent subject matter, restriction for examination purposes as indicated is proper.

1.3 On 8 March 2004, Examiner telephoned Applicant's attorney, Ms. Ann McCrackin, Reg. No. 42,858, regarding an election/restriction requirement. Ms. McCrackin agreed to elect claims 1-6, 16-20, and 21-25 without traverse. Applicant is requested to formally cancel claims 7-15 as part of any response to this office action.

2. Claims 1-6, 16-20, and 21-25 have been examined.

Information Disclosure Statement

3. Page 1 of the Specification lists the following publications as prior art:

1. Van Genderen, "Network Initialization in a Switch-Level Simulator"; and
2. Wehbeh et al, "On the Initialization of Sequential Circuits."

The Examiner was able to locate the publication by Van Genderen and it is listed on Form PTO-892 "Notice of References Cited" included with this Office Action. The Examiner was unable to locate the publication by Wehbeh et al and requests the Applicant supply it in a Supplemental

Information Disclosure Statement. It is unclear why these publications were referenced in the Application but omitted from Applicant's Information Disclosure Statement submitted as Paper No. 2.

Applicant is reminded of the duty under MPEP Paragraphs 2000.01 - 2022.05 to disclose any material prior art known at the time of filing.

Drawings

4. This application has been filed with informal drawings which are acceptable for examination purposes only. Formal drawings will be required when the application is allowed.

Claim Rejections - 35 U.S.C. § 101

5. The following is a quotation of 35 U.S.C. 101:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5.1 Claims 21-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

5.2 Regarding independent claim 21, this claim recites in-part: "An article having a computer readable medium, the computer readable medium comprising a **data structure** describing a device model for use in a simulator, . . ." (Emphasis added.) The remainder of the claim does not define any structural and functional interrelationships between the computer

readable medium and a computer that permits the article's functionality to be realized. Therefore, claim 21 represents non-statutory descriptive material; see MPEP Section 2106, subsection IV.B.1(a).

5.3 Claims 22-25 are dependent on claim 21 and rejected using the same analysis.

Claim Rejections - 35 U.S.C. § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> . . .
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6.1 Claims 1-6 and 16-25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Smith, "Set-and-See Switch-Level Simulation for VLSI Functional Verification," IEEE 39th Midwest Symposium on Circuits and System, Vol. 1 pp. 402-405 (August 1996).

6.2 Smith teaches the combination of the "Magic" VLSI layout editor with the "Esim" switch-level simulator. See pages 402-3. Name and geometry attributes for each node in a circuit are stored in a table and initially unknown values are "painted" on all nodes but power and ground. The user then sets values to one or zero; see page 404 column 1 paragraphs 3-4.

6.3 Regarding claims 1-3 and 5, the user operating the "Set-and-See" simulator conditionally treats unknown node input states as known values when initializing the simulation, evaluates the resulting output nodes by using the "known" input states, including by setting one or more input nodes as a "0."

6.4 Regarding claims 5 and 6, Smith also teaches use of the "Set-and-See" simulator to model a CMOS inverter including a switch-level model of a transistor, including detecting an X on the input node and evaluating the output node to a "1"; this result occurs by definition when the user sets the input node to "0." Similarly, the detection of on X on the input node and then evaluating the output node to "0" occurs by definition with the user sets the input node to "1." See "SCMOS Inverter" pages 404-5 starting at column 2 paragraph 5.

6.5 Regarding claims 16-25, these claims are anticipated using the analysis of claims 1-6 above, in conjunction with the "logging file" that permits the user to conditionally treat unknown input nodes. See "Modifications to the Simulator" pages 403-4 starting at column 2 paragraph 5.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to Applicant's disclosure. Reference to Williams et al, U.S. Patent 5,991,523, is cited as teaching a method and system for hdl global signal simulation using a "STARTBUF" cell.

Reference to Bening, "A Two-State Methodology for RTL Logic Simulation," Proceedings of the 36th Design Automation Conference, pp. 672-677 (June 1999), is cited as teaching an RTL logic simulation using random two-state initialization to eliminate X-states.

Reference to Maxfield, "'Xs' in Digital Simulation: Beware, Here be Dragons," EDN Access, downloaded text from http://www.e-insite.net/ednmag/archives/1995/101295/21df4.htm (October 1995), is cited as teaching using an internal simulator function to randomly coerce uninitialized "X" values into logic 0s and logic 1s. See downloaded text at pages 6-7.

Reference to Van Genderen, "Network Initialization in a Switch-Level Simulator," Proceedings of the 1995 European Design and Test Conference, p. 596 (March 1995), is cited as teaching user-defined and random initialization techniques for switch-level simulators.

Reference to Anonymous, "IEEE Standard Multivalue Logic System for VHDL Model Interoperability (Std_logic_1164)," IEEE Standards Board, pp. 1-17 (March 1993), is cited as teaching a standard of handling 'unknown' and 'don't care' values in VHDL programs.

Reference to Cheng et al, "A Sequential Circuit Test Generator Using Threshold-Value Simulation," 18th International Symposium on Fault-Tolerant Computing", pp. 24-29 (June 1988), is cited as teaching using a threshold value model to propagate unknown values through circuits to generate tests for both synchronous and asynchronous circuits.

8. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Samuel Broda, whose telephone number is (703) 305-1026. The Examiner can normally be reached on Mondays through Fridays from 8:00 AM – 4:30 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Kevin Teska, can be reached at (703) 305-9704. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the group receptionist, whose telephone number is (703) 305-3900.

SAMUEL BRODA, ESQ.
PRIMARY EXAMINER